

Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain — Min $h_{FE} = 1000$ @ $I_C = 5$ A, $V_{CE} = 4$ V
- Collector–Emitter Sustaining Voltage — @ 30 mA
 $V_{CE(sus)} = 60$ Vdc (Min) — TIP140, TIP145
 80 Vdc (Min) — TIP141, TIP146
 100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor

MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 15			A dc
Base Current — Continuous	I_B	0.5			A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

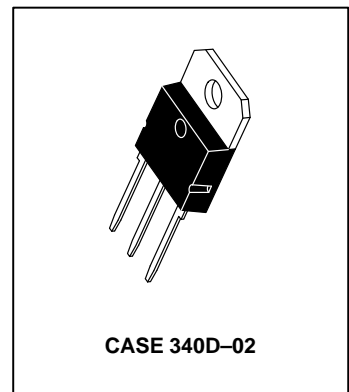
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C}/\text{W}$
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C}/\text{W}$

(1) 5 ms, $\leq 10\%$ Duty Cycle.

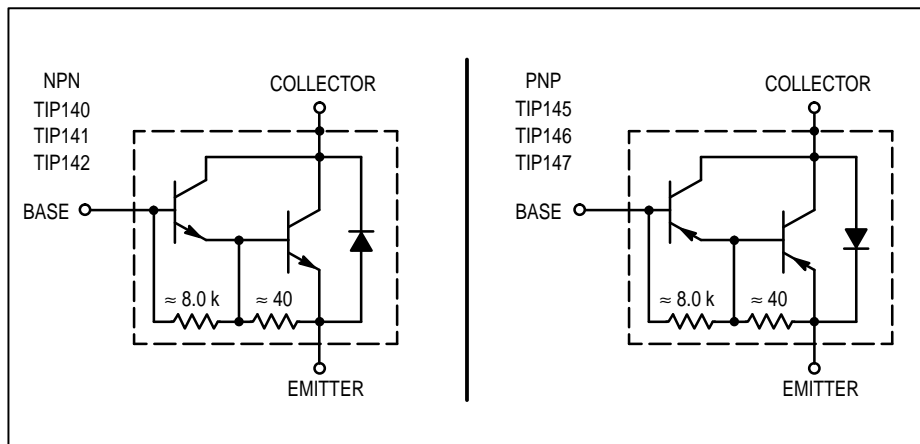
NPN
TIP140
TIP141*
TIP142*
PNP
TIP145
TIP146*
TIP147*

*Motorola Preferred Device

10 AMPERE
DARLINGTON
COMPLEMENTARY SILICON
POWER TRANSISTORS
60–100 VOLTS
125 WATTS



DARLINGTON SCHEMATICS



Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

TIP140 TIP141 TIP142 TIP145 TIP146 TIP147

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	60 80 100	— — —	— — —	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	— — —	— — —	2.0 2.0 2.0	mA
Collector Cutoff Current ($V_{CB} = 60\text{ V}$, $I_E = 0$) ($V_{CB} = 80\text{ V}$, $I_E = 0$) ($V_{CB} = 100\text{ V}$, $I_E = 0$)	I_{CBO}	— — —	— — —	1.0 1.0 1.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ V}$)	I_{EBO}	—	—	2.0	mA

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 5.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	1000 500	— —	— —	—
Collector–Emitter Saturation Voltage ($I_C = 5.0\text{ A}$, $I_B = 10\text{ mA}$) ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{CE(sat)}$	— —	— —	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{BE(sat)}$	—	—	3.5	Vdc
Base–Emitter On Voltage ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	—	—	3.0	Vdc

SWITCHING CHARACTERISTICS

Resistive Load (See Figure 1)						
Delay Time	$V_{CC} = 30\text{ V}$, $I_C = 5.0\text{ A}$, $I_B = 20\text{ mA}$, Duty Cycle $\leq 2.0\%$, $I_{B1} = I_{B2}$, R_C & R_B Varied, $T_J = 25^\circ\text{C}$	t_d	—	0.15	—	μs
Rise Time		t_r	—	0.55	—	μs
Storage Time		t_s	—	2.5	—	μs
Fall Time		t_f	—	2.5	—	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

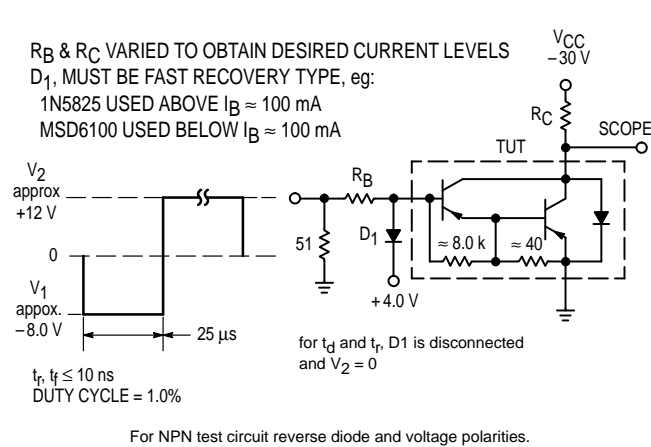


Figure 1. Switching Times Test Circuit

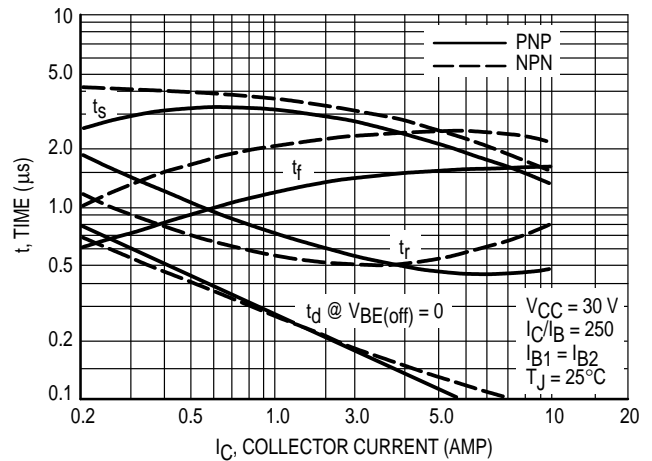


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

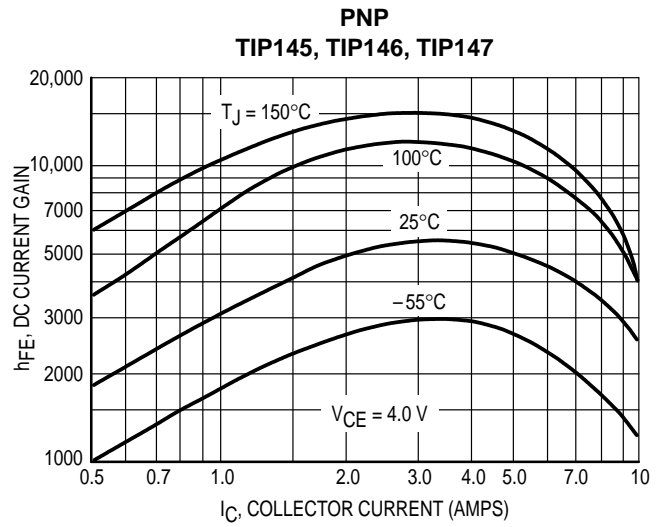
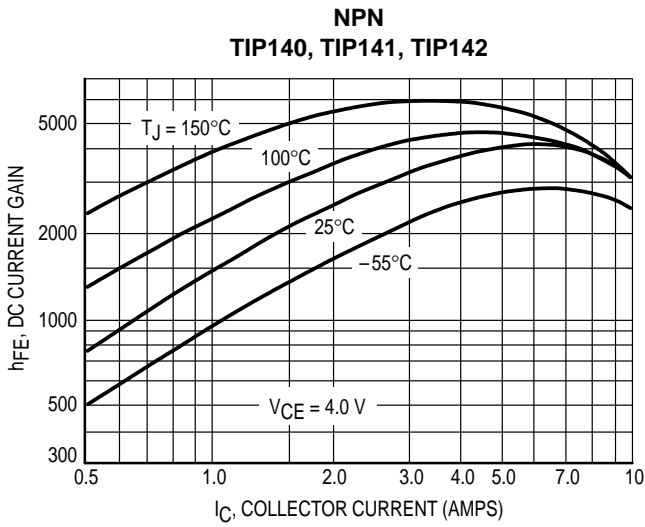


Figure 3. DC Current Gain versus Collector Current

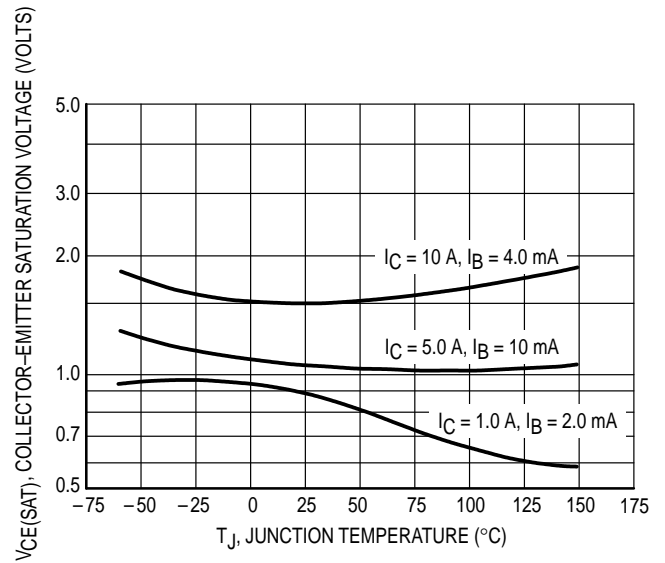
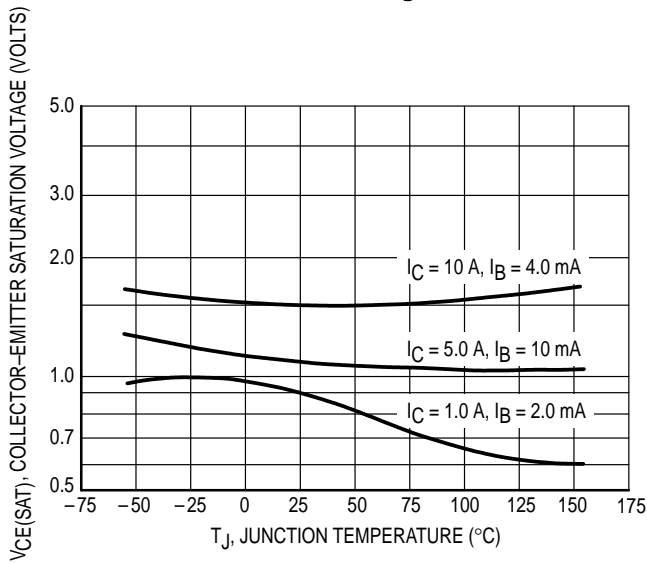


Figure 4. Collector-Emitter Saturation Voltage

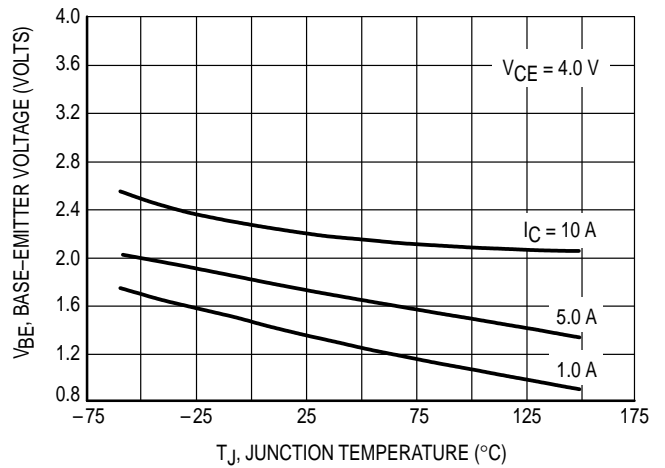
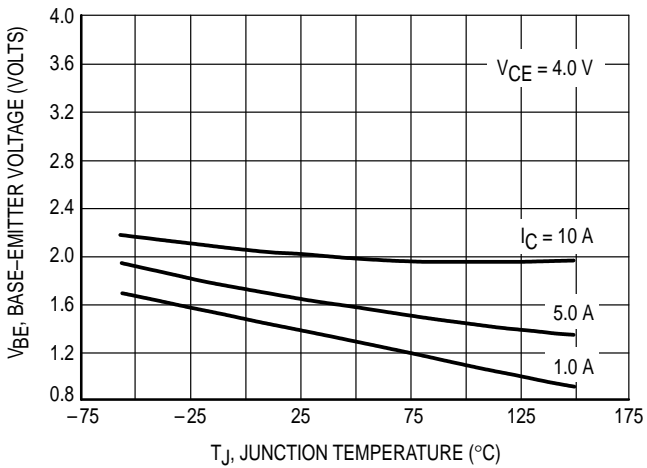


Figure 5. Base-Emitter Voltage

ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

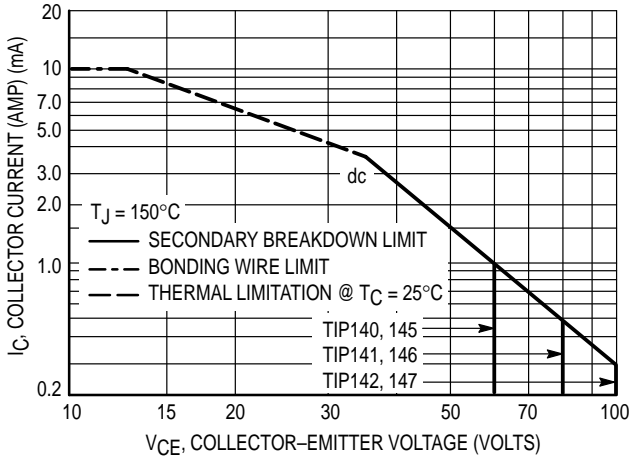


Figure 6. Active-Region Safe Operating Area

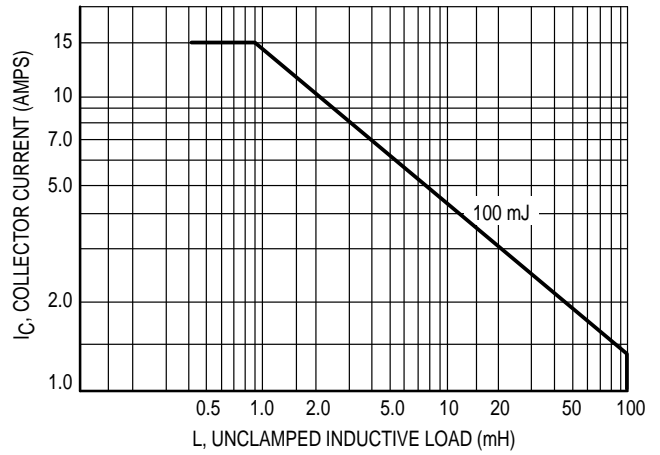
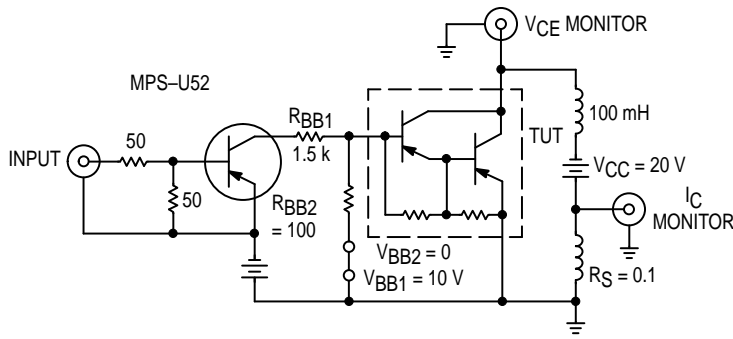
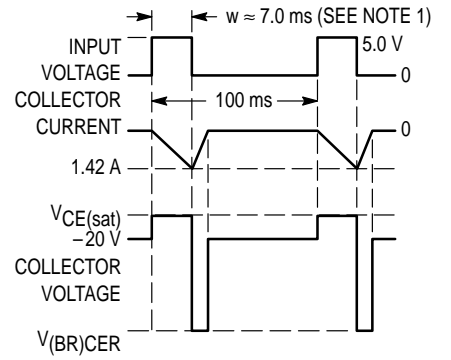


Figure 7. Unclamped Inductive Load



TEST CIRCUIT

NOTE 1: Input pulse width is increased until $I_{CM} = 1.42\text{ A}$.
NOTE 2: For NPN test circuit reverse polarities.



VOLTAGE AND CURRENT WAVEFORMS

Figure 8. Inductive Load

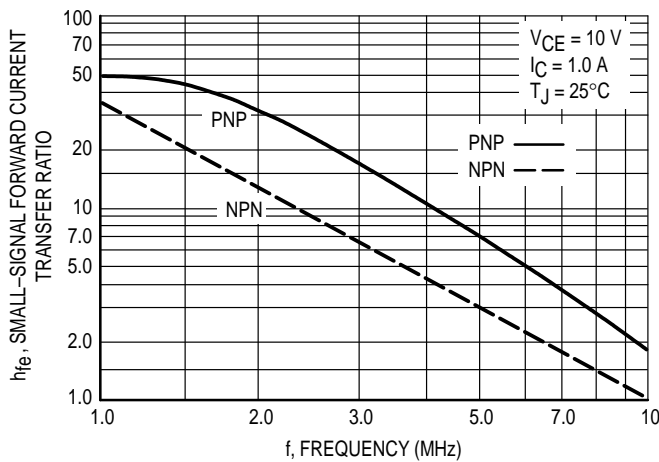


Figure 9. Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio

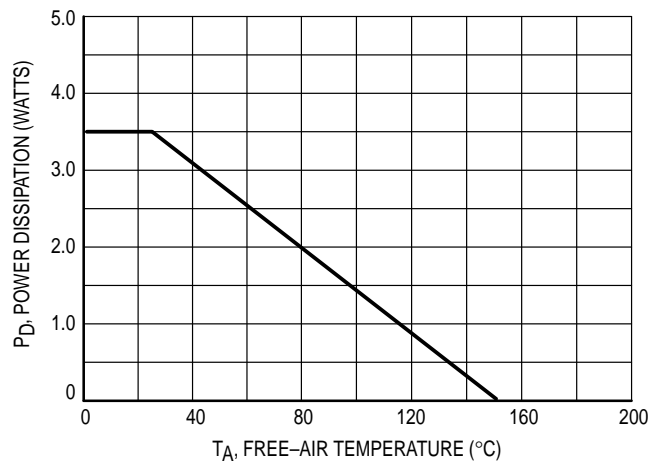
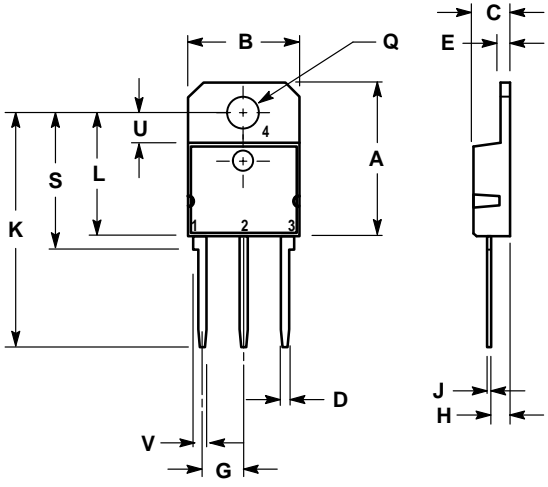


Figure 10. Free-Air Temperature Power Derating

PACKAGE DIMENSIONS




NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	20.35	—	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	—	16.20	—	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 340D-02
 ISSUE B

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